CLAIMS

What is claimed is:

1. A method for aligning a semiconductor device with a carrier substrate for electrical interconnection therebetween, the method comprising:

forming at least two apertures through the semiconductor device from a first major surface thereof to a second and opposing major surface thereof;

providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two apertures;

placing the semiconductor device over the carrier substrate; and

aligning the at least two apertures formed in the semiconductor device with the at least two alignment features of the carrier substrate.

2. The method of claim 1, wherein aligning the at least two apertures with the at least two alignment features includes sighting each alignment feature through a respective corresponding aperture.

3. The method of claim 1, wherein providing the carrier substrate with at least two alignment features includes forming at least two holes in the carrier substrate.

4. The method of claim 3, wherein forming the at least two holes in the carrier substrate includes forming at least two blind holes therein.

5. The method of claim 3, wherein aligning the at least two apertures with the at least two alignment features includes placing pins through the at least two apertures and into the at least two holes.

6. The method of claim 5, further comprising forming the pins of a non-conductive material.

7. The method of claim 5, further comprising forming the pins of an anti-static material.

8. The method of claim 5, further comprising affixing the pins to the semiconductor device and to the carrier substrate.

9. The method of claim 8, wherein affixing the pins to the semiconductor device and to the carrier substrate includes thermally bonding the pins to the semiconductor device and to the carrier substrate.

10. The method of claim 5, further comprising forming the pins with a mechanical self-locking mechanism proximate at least one end thereof.

11. The method of claim 5, further comprising removing the pins subsequent to the alignment of the at least two apertures with the at least two alignment features.

12. The method of claim 3, wherein placing the semiconductor device on the carrier substrate is effected using a pick and place device.

13. The method of claim 12, wherein the pick and place device is used to align the semiconductor device with the carrier substrate by inserting pins carried by a head of the pick and place device through the at least two apertures and the at least two holes.

14. The method of claim 13, further including lifting the pick and place device including the locating pins from the aligned semiconductor device and carrier substrate.

15. The method of claim 1, wherein providing at least two alignment features in the carrier substrate includes forming at least two pins on the carrier substrate.

16. The method of claim 15, wherein forming at least two pins on the carrier substrate includes forming a mechanical locking mechanism proximate an end of each of the at least two pins.

17. The method of claim 1, wherein providing at least two alignment features in the carrier substrate includes forming optically perceptible marks on the carrier substrate.

18. The method of claim 17, further comprising aligning the at least two apertures with the at least two alignment features by sighting the optically perceptible marks on the carrier substrate through the at least two apertures of the semiconductor device.

19. The method of claim 18, wherein sighting the optically perceptible marks on the carrier substrate through the at least two apertures includes sighting the optically perceptible marks with an optical instrument.

20. The method of claim 1, wherein the at least two apertures are each defined by a diameter and wherein the method further comprises forming at least one of the at least two apertures with a larger diameter than that of at least one other aperture of the at least two apertures.

21. The method of claim 20, wherein providing at least two alignment features on the carrier substrate includes correlating a size of each of the at least two alignment features with a size of each of a respectively corresponding aperture.

22. The method of claim 1, wherein forming the at least two apertures includes forming the at least two apertures in an asymmetrical pattern on the semiconductor device.

23. The method of claim 1, wherein forming the at least two apertures includes forming at least one notch on a periphery of the semiconductor device.

24. A method of testing a semiconductor device having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising:

providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements;

forming at least two apertures in the semiconductor device, each aperture passing from a first surface to a second opposing surface thereof;

providing the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two apertures;

placing the semiconductor device over the carrier substrate;

aligning each aperture formed in the semiconductor device with a respectively corresponding alignment feature of the carrier substrate;

electrically contacting each discrete conductive element with a terminal pad; and

passing at least one electrical signal between the semiconductor device and the carrier substrate.

25. The method of claim 24, wherein aligning the at least two apertures with the at least two alignment features includes sighting each alignment feature through a respectively corresponding aperture.

26. The method of claim 24, wherein providing the carrier substrate with at least two alignment features includes forming at least two holes in the carrier substrate.

27. The method of claim 26, wherein forming at least two holes in the carrier substrate includes forming at least two blind holes.

28. The method of claim 26, wherein aligning the at least two apertures with the at least two alignment features includes placing pins through the at least two apertures and into the at least two holes.

29. The method of claim 28, further comprising forming the pins of a non-conductive material

30. The method of claim 28, further comprising forming the pins of an anti-static material.

31. The method of claim 28, further comprising affixing the pins to the semiconductor device and to the carrier substrate.

32. The method of claim 31, wherein affixing the pins to the semiconductor device and to the carrier substrate includes thermally bonding the pins to the semiconductor device and the carrier substrate.

33. The method of claim 29, further comprising forming a mechanical self-locking mechanism proximate at least one end thereof.

34. The method of claim 29, further comprising removing the pins subsequent to the alignment of the at least two apertures with the at least two alignment features.

35. The method of claim 27, wherein placing the semiconductor device on the carrier substrate includes is effected using a pick and place device.

36. The method of claim 35, wherein the pick and place device is used by placing pins carried by a head of the pick and place device through the at least two apertures and the at least two holes.

37. The method of claim 36, further including lifting the pick and place device including the locating pins from the aligned semiconductor device and carrier substrate.

38. The method of claim 25, wherein providing at least two alignment features in the carrier substrate includes forming pins on the carrier substrate.

39. The method of claim 38, wherein forming pins on the carrier substrate includes forming a mechanical locking mechanism proximate end of the pins.

40. The method of claim 25, wherein providing at least two alignment features in the printed circuit board includes forming at least two optically perceptible marks on the carrier substrate.

41. The method of claim 40, further comprising aligning the at least two apertures with the at least two alignment features by sighting the at least two optically perceptible marks on the carrier substrate through the at least two apertures of the semiconductor device.

42. The method of claim 41, wherein sighting the at least two optically perceptible marks one the carrier substrate through the at least two apertures is effected using an optical instrument.

43. The method of claim 25, wherein the at least two apertures are each defined by a diameter and wherein the method further comprises forming at least one of the at least two apertures with a larger diameter than that of at least one other aperture.

44. The method of claim 43, wherein providing at least two alignment features on the printed circuit board includes correlating a size of each alignment feature with a size of a respectively corresponding aperture.

45. The method of claim 25, wherein forming the at least two apertures includes forming the at least two apertures in an asymmetrical pattern on the semiconductor device.

46. The method of claim 25, wherein forming the at least two apertures includes forming at least one notch on a periphery of the semiconductor device.

47. An alignment tool for aligning a semiconductor device with a carrier substrate comprising:

a head including a holding mechanism including structure for releasably holding a semiconductor device;

an alignment structure carried at least in part by the head, associated with the holding mechanism and configured to effect alignment of at least two apertures formed through a semiconductor device with at least two corresponding alignment features formed on a carrier substrate when the semiconductor device is superimposed over the carrier substrate.

48. The alignment tool of claim 47, wherein the alignment features comprise holes formed in the carrier substrate and wherein the alignment structure includes at least two pins carried by the head, the at least two pins being configured, spaced and positioned for insertion through the at least two apertures and into the at least two corresponding holes.

49. The alignment tool of claim 48, wherein the structure for releasably holding the semiconductor device includes a suction device positioned to attach to a surface of the semiconductor device.

50. The alignment tool of claim 47, wherein the head and the at least two pins are configured for removal of the at least two pins from the alignment tool after insertion of the pins through the at least two apertures of the semiconductor device and the at least two holes of the carrier substrate.

51. The alignment tool of claim 50, wherein the at least two pins include a mechanical locking device proximate at least one end of each pin.

52. The alignment tool of claim 50, wherein the at least two pins are adapted to be thermally bonded to at least one of the semiconductor device and the carrier substrate.

53. The alignment tool of claim 52, wherein the at least two pins are adapted to be thermally bonded to both the semiconductor device and the carrier substrate.

54. The alignment tool of claim 47, wherein the at least two pins are fixed to the alignment tool.

55. The alignment tool of claim 47, wherein the at least two pins each have a diameter, and wherein one of the at least two pins has a larger diameter than at least one other pin of the at least two pins.

56. The alignment tool of claim 47, wherein the at least two pins are arranged asymmetrically.

57. The alignment tool of claim 47, wherein the at least two alignment features comprise optically perceptible markings and wherein the alignment structure is adapted to optically detect the optically perceptible markings.

58. The alignment head of claim 57, wherein the alignment structure is located and adapted to detect the optically perceptible marks by sighting through the at least two apertures when the semiconductor device is held by the holding mechanism.

59. A semiconductor device assembly, comprising:

at least one semiconductor device having at least two apertures extending therethrough; and

a carrier substrate having at least two alignment features thereon spaced and positioned in correspondence to spacing and positioning of the at least two apertures, the at least one semiconductor device superimposed over the carrier substrate with the at least two apertures aligned with the at least two alignment features.

60. The semiconductor device assembly of claim 59, further comprising structure securing the at least one semiconductor device to the carrier substrate.

61. The semiconductor device assembly of claim 60, wherein the structure securing the at least one semiconductor device to the carrier substrate comprises pins inserted through the at least two apertures and secured to the carrier substrate.

62. The semiconductor device assembly of claim 61, wherein the at least two alignment features comprise holes, and the pins are received in the holes.